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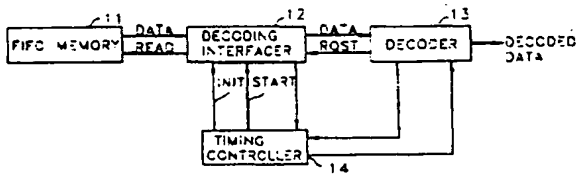
(54) Variable-length decoder for bit-stuffed data.

(57) A variable-length decoder decodes a bit-stuffed bitstream received. Variable-length-encoded data is bit-stuffed in each data block to become a predetermined number of bits, and a frame start code representing a start of one frame and a mass of macroblock (MMB) start code for discriminating a plurality of the MMBs contained in one frame from one another is inserted and transmitted in the form of the bitstream. A first-in-first-out (FIFO) memory (11) stores the transmitted data and sequentially outputs a predetermined number of bits of data starting from firstly stored bits every time a read signal is input thereto. A decoder (13) variable-length-decodes the input data in response to a control signal, generates a data request signal every time the number of bits of the data used for a variable-length-decoding operation becomes a predetermined number of bits, and generates an end-of-block (EOB) error signal when the EOB data does not exist every data interval. A decoding interfacer (12) generates the read signal in response to a start signal and the data request signal which is output from the decoder means (13) to then be supplied to the FIFO memory (11), stores the data applied from the FIFO memory (11) according to the read signal by a predetermined number of bits, interrupts generation of the read signal if one of the frame start code and the MMB start code is detected from the input data, and supplies the stored data to the decoder (13) by a predetermined number of bits if an initialization signal is input. A timing controller (14) generates the start signal every frame interval and the initialization signal every MMB interval to be supplied to the decoding interfacer (12), generates a new start signal to be supplied to the decoder (13) if the EOB error signal is input and generates a signal for controlling the variable-length-decoding operation to be supplied to the decoder (13).

FIG. 5



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The present invention relates to a variable-length decoder, and more particularly, though not exclusively, to a variable-length decoder for variable-length-decoding variable-length-encoded and bit-stuffed data.

Generally, digital video signal encoding methods are divided into a signal source encoding method and an entropy encoding method. The signal source encoding method uses redundancy contained in a video signal to compress video data, for which a discrete cosine transform (DCT) method, a band-division encoding method and a differential pulse code modulation (DPCM) method are used. The entropy encoding method compresses further the data compressed by the signal source encoding method based on statistical occurrence frequency for which a variable-length coding (VLC) method is representatively used. The VLC method is usually composed of a run-length coding method and a (modified) Huffman coding method. Here, a pair of "run" and "level" obtained by the run-length coding method is considered as a single symbol. Accordingly, a shorter codeword is assigned to a symbol having higher occurrence frequency in the Huffman code table. On the other hand, a relatively longer codeword is assigned to the other symbol having lower occurrence frequency in the Huffman code table. Thus, the total data transmission rate is reduced. Such encoding methods are being used in a digital high-definition television (HD-TV) such as an advanced TV in U.S.A., and the Moving Picture Expert Group (MPEG) of which the standardization is pursued in the ISO/CCITT.

The digital HD-TV system uses a combination of the signal source encoding method and the VLC method which adopt the DCT or DPCM. Also, since an amount of the data to be processed is extremely large, a picture is divided into several windows to then be processed, of which one example will be described below with reference to Figures 1 and 2.

Figure 1 shows an encoding system for video data and Figure 2 shows a decoding system for video data. When the systems of Figures 1 and 2 are used, a picture can be divided into four windows to then be processed, thereby lowering a processing speed of video data. In the encoding system of Figure 1, input video data is divided into data of four channels by a channel divider 1, the divided channel data is compressed by each signal source encoder 2A, 2B, 2C or 2D. The video data compressed by signal source encoders 2A through 2D is further compressed by variable-length encoders 3A through 3D. The data output from variable-length encoders 3A through 3D is applied to a multiplexer 4. Multiplexer 4 multiplexes the input data to produce an encoded bitstream.

The decoding system of Figure 2 restores the bitstream produced by the Figure 1 system into the prior-to-being-encoded video data. An inverse multiplexer 5 separates the input bitstream into the data of the four channels. Each of variable-length decoders 6A through 6D variable-length-decodes the separated channel bitstream and each of signal source decoders 7A through 7D decodes the variable-length-decoded data to generate data substantially same as that of the prior-to-being-encoded video data in the corresponding channel. A multiplexer 8 multiplexes the respective window data output from signal source decoders 7A through 7D to generate decoded video data. As a result, the data output from multiplexer 8 becomes data substantially the same as that applied to channel divider 1 of Figure 1.

Figure 3 shows that one frame picture is divided into four windows. One window is composed of fifteen sets of a mass of macroblocks (MMBs). One MMB is composed of four slices. One slice of a plurality of macroblocks. When the system of Figure 1 uses a data structure shown in Figure 3, the system multiplexes the video data in units of the MMB. Thus, signal source encoder 2A and variable-length encoder 3A processes the MMBs in the first window, that is, MMB1, MMB5, ... and MMB57. Multiplexer 4 multiplexes the data belonging to the four windows in the order of MMB1, MMB2, MMB3, MMB4, MMB5, ... and MMB60. The system of Figure 2 separates the encoded bitstream into the video data of each window via an inverse procedure of the multiplexing process of the Figure 1 system, and variable-length-decodes and signal-source-decodes the separated video data in each window.

By the way, when the video data is transmitted from the Figure 1 system in a constant transmission rate via a buffer (not shown), an amount of the data generated by the signal source encoders and the variable-length encoders is not constant, a bit stuffing operation is performed in the variable-length-encoded data block, to solve such a problem. The bit stuffing operation stuffs bits which are not filled with video information or codes for discriminating the data blocks from each other among the bits determined with respect to data blocks, with meaningless information, for example, consecutive zeros. Thus, an actual variable-length decoder 6A, 6B, 6C or 6D receives data which is obtained by variable-length-encoding and bit-stuffing the encoded bitstream. The variable-length-decoder 6A, 6B, 6C or 6D includes a first-in-first-out (FIFO) memory and a variable-length decoder unit. The variable-length decoder unit reads out a predetermined number of bits of data from the FIFO memory to perform a variable-length decoding operation and determine whether a predeter-

mined number of following bits of data will be read out on the basis of the number of the bits of which the variable-length-decoding operation is finished. Therefore, when the bit-stuffed bits are read out from the FIFO memory, the variable-length decoder cannot perform any variable-length decoding operation with respect to such bits. Accordingly, it becomes difficult in reading a predetermined number of the following bits and it becomes also difficult in variable-length-decoding the bits following the bit-stuffed data.

Moreover, when an error is generated in the bitstream during transmission, the variable-length decoder performs a wrong variable-length decoding operation with respect to the error-generated bits. When a degree of the error is severe. data is wrongly read from the FIFO memory, thereby wrongly decoding the bits following the error-generated bit.

The above-described problems cause sync collapse between the decoded data corresponding to the respective windows, when one picture is divided into four windows.

It is an aim of preferred embodiments of the present invention to provide a variable-length decoding apparatus in which a frame start code and a mass of macroblock (MMB) start code are used to control a reading operation of variable-length-encoded data from a FIFO memory, and the data read from the FIFO memory by such a control is variable-length-decoded.

According to the present invention, there is provided a variable-length decoding apparatus for variable-length-decoding data transmitted in the form of bitstream after bit-stuffing variable-length-encoded data in each data block to become a predetermined number of bits, and inserting a frame start code representing a start of one frame and a mass of macroblock (MMB) start code for discriminating a plurality of the MMBs contained in one frame from one another, the variable-length decoding apparatus comprising:

a first-in-first-out (FIFO) memory for storing transmitted data and sequentially outputting a predetermined number of bits of data starting from firstly stored bits every time a read signal is input thereto;

decoder means for variable-length-decoding the input data in response to a control signal, generating a data request signal every time the number of bits of the data used for a variable-length-decoding operation becomes a predetermined number of bits, and generating an end-of-block (EOB) error signal when the EOB data does not exist every block data interval;

decoding interface means for generating the read signal in response to a start signal and the data request signal which is output from the decoder means to then be supplied to the FIFO memory, storing the data applied from the FIFO memory according to the read signal by a predetermined number of bits, interrupting generation of the read signal if one of the frame start code and the MMB start code is detected from the input data, and supplying the stored data to the decoder means by a predetermined number of bits if an initialization signal is input; and

a timing controller for generating the start signal every frame interval and the initialization signal every MMB interval to be supplied to the decoding interface means, generating a new start signal to be supplied to the decoder means if the EOB error signal is input, and generating a signal for controlling the variable-length-decoding operation to be supplied to the decoder means.

Suitably, wherein said decoding interface means comprises:

a data latch portion of which the data input end is connected to a data output end of said FIFO memory, and of which the data output end is connected to said decoding means, for latching the data output from said FIFO memory by a predetermined number of bits every read signal, to twice the predetermined number of bits in the input order according to a select signal;

a detector for receiving the data latched to said data latch portion and the data output from said FIFO memory, detecting one between the frame start signal and the MMB start signal, latching a first binary signal which is generated to vary the value thereof according to a detection result, and clearing the latched first binary signal if one among the start signal and the initialization signal is input from said timing controller; and

a control signal generator for generating the read signal of which the value one between the first binary value for enabling to read the data from said FIFO memory and a second binary value for disabling the read of the data from said FIFO memory, and the select signal of which the value is one between a third binary value for newly latching the data supplied from said FIFO memory and a fourth binary value for maintaining the already-latched data as it is.

Suitably, said data latch portion comprises:

first and second latches for sequentially latching the data output from said FIFO memory by predetermined bits and outputting the latched data to said decoding means;

a first multiplexer for receiving the output data from said FIFO memory and said first latch and outputting the received data to said first latch according to a binary value of the select signal; and

a second multiplexer for receiving the output data from said first and second latches and outputting the received data to said second latch accord-

ing to a binary value of the select signal.

Suitably, said detector comprises:

third and fourth latches of which the output values are cleared into zero respectively by the start signal and the initialization signal from said timing controller;

a first comparator for comparing the output data from said first latch with the predeterminedly set MMB start code, and outputting a first binary signal having a binary value of "1" if the data is identical to each other according to the comparison result while outputting the first binary signal having a binary value of "0" if the data is different from each other according to the comparison result;

a second comparator for comparing the data input to said first multiplexer with a part of the predeterminedly set frame start code, and outputting a second binary signal having a binary value of "1" if the data is identical to each other according to the comparison result while outputting the first binary signal having a binary value of "0" if the data is different from each other according to the comparison result;

a third multiplexer for selecting one between the output data of said third latch and said first comparator according to the select signal and outputting the selected result to said third latch;

a fourth multiplexer for selecting one between the output data of said fourth latch and said second comparator according to the select signal and outputting the selected result to said fourth latch; and

a fifth latch for latching the output data from said third latch.

Suitably, said control signal generator comprises:

an RS flip-flop for receiving the start signal from said timing controller via one input end (S) and the first binary signal from said third latch via another input end (R), and outputting the data via the output end (Q);

an AND gate for logically multiplying the data request signal from said decoding means by an inverted output data of said fifth latch;

an OR gate for logically summing the output data from said RS flip-flop and the output data from said AND gate and outputting the logically summed result;

a sixth latch for latching the output from said OR gate and outputting the latched result as the read signal applied to said FIFO memory; and

a seventh latch for latching the output data from said sixth latch and outputting the latched result as the select signal.

Suitably, said decoding interface means generates a detection resultant signal if the frame start code is detected and outputting the generated signal to said timing controller, and

wherein said timing controller outputs the start signal for the first operation of said variable-length decoding apparatus to said decoding interface means, generates a new start signal to read the data containing the MMB start code from said FIFO memory based on a detection resultant signal if the detection resultant signal is applied from said decoding interface means in response to the start signal for the first operation, and outputs the generated new start signal to said decoding interface means.

According to another aspect of the present invention, there is provided a variable length decoding apparatus comprising means for generating a read signal to output data from a memory means, in which generation of the read signal is interrupted if one of a frame start code or a macroblock code is detected.

Suitably, said apparatus further comprises any one or more of the features disclosed in the accompanying specification, claims, abstract and/or drawings, in any combination.

Preferred embodiments of the present invention are described, by way of example only, with reference to the drawings wherein:

Figure 1 is a block diagram of a general video signal encoding system.

Figure 2 is a block diagram of a general video signal decoding system.

Figure 3 is a view for explaining an example of a processing unit of video data according to the present invention.

Figures 4A and 4B are views showing an example of a bitstream proposed in the present invention to decode bit-stuffed bitstream.

Figure 5 is a block diagram of a variable-length decoding apparatus according to a preferred embodiment of the present invention.

Figure 6 is a circuit diagram showing an example of the detailed construction of the decoding interface of Figure 5.

A preferred embodiment of the present invention will be described below in more detail with reference to the accompanying drawings Figures 4A through 6.

Figures 4A and 4B show a structure of a bitstream used in a preferred embodiment of the present invention. Figure 4A shows a structure of a bitstream belonging to one frame. The bitstream of Figure 4A is constructed to be adapted in a case where a FIFO memory for a variable-length-decoding operation outputs 24-bit data basically. It is apparent that a number of modifications are possible within the scope of the present invention for performing a variable-length-decoding operation with respect to the number of bits different from the 24 bits. The bitstream of Figure 4A can be a structure of the bitstream corresponding to each window which is separated by inverse multiplexer

5, or that corresponding to one frame prior to being separated. The one-frame bitstream includes frame head data comprising a frame start code (FSC), a frame number (FN), buffer status information (BSI) and stuffed bits. In a preferred embodiment of the present invention, the number of bits of the FSC is 32, that of the FN is 4, that of the BSI is 20 and that of the stuffed bits are 16. Fifteen or sixty MMBs are located at the rear end of the stuffed bits. One frame is composed of sixty MMBs. If one frame is divided into four windows, fifteen MMBs are contained in each window every frame. Each MMB is composed of MMB head data having a 24-bit MMB start code (MSC) and an 8-bit MMB number (MN) and the stuffed bits. Four q-levels, eleven macroblock, head information and macroblock data are located between the MN and the stuffed bits. The macroblock head information includes field/frame information, a macroblock q-level (mquant), inter/intra information, a horizontal motion vector (X-MV) and a vertical motion vector (Y-MB). Each block also includes a DCT coefficient (dct_coeff) and an end-of-block (EOB) representing the end of the block. Here, the FSC, the frame number the MSC and the MMB number (or the MMB address) use a fixed-length code, respectively. Since the number of bits of the other codes is varied as is the case, a bit of "0" for bit-stuffing is added by the insufficient number of bits when the MMB data does not become a multiple of 24 bits.

Figure 5 is a block diagram of a variable-length decoding apparatus according to a preferred embodiment of the present invention. The Figure 5 apparatus variable-length-decodes input data based on a basic data format with respect to bit-stuffed data after being variable-length-encoded. In Figure 5, a FIFO memory 11 stores bitstream corresponding to one window described in relation to Figures 4A and 4B. Whenever a read signal is input, 24-bit data starting from firstly stored bits is output to a decoding interfacer 12. The decoding interfacer 12 detects an FSC or an MSC from the data read from FIFO memory 11 to output the detection resultant signal to a timing controller 14. The decoding interfacer 12 transmits also the data read out from FIFO memory 11 to decoding unit 13. Decoding unit 13 variable-length-decodes the data supplied from decoding interfacer 12 and generates a data request signal RQST to be supplied to decoding interfacer 12. Decoding unit 13 generates also an EOB error signal according to detection of an EOB signal representing the end of each block, and supplies the generated EOB error signal to timing controller 14. Timing controller 14 generates an initialization signal (INIT) and a start signal to be supplied to decoding interfacer 12, and generates a control signal necessary for a variable-length-decoding operation to be supplied to decoding unit 13.

The operation of the Figure 5 apparatus having the above-described construction will be described below.

When the Figure 5 apparatus operates for the first time, timing controller 14 generates that start signal so as to start to process the one-frame data, and supplies the generated start signal to decoding interfacer 12. Decoding interfacer 12 generates the read signal in response to the start signal to output the same to FIFO memory 11. FIFO memory 11 receives the data corresponding to one window among four windows constituting one frame in the form of bitstream and stores the received data, and outputs 24-bit data to decoding interfacer 12 starting from the firstly stored data whenever the read signal is applied thereto. Decoding interfacer 12 latches the data read from FIFO memory 11 every 72-bit data, and uses the latched data to detect the FSC. When the FSC is detected, decoding interfacer 12 outputs the detection resultant signal to timing controller 14. When the detection resultant signal is applied thereto, timing controller 14 generates a new start signal. The new start signal is used for reading the data following the 72-bit data latched by decoding interfacer 12. Timing controller 14 generates also a signal for controlling a data decoding operation for data which is supplied from FIFO memory 11 to decoding unit 13 to supply the generated signal to decoding unit 13. Decoding interfacer 12 reads data from FIFO memory 11 in response to the new start signal and detects an MSC using the read data. The detection resultant signal according to the detection of the MSC is supplied to timing controller 14. Timing controller 14 generates an initialization signal INIT in response to the detection resultant signal. The initialization signal INIT is generated in timing controller 14 at the previous point of time from the point of time when the respectively variable-length encoded data of the MMBs is read from FIFO memory 11. Decoding interfacer 12 reads data from FIFO memory 11 according to data request signal RQST which is applied from decoding unit 13 if the initialization signal is applied. Decoding unit 13 variable-length-decodes the data supplied from decoding interfacer 12 using an internal decoding table, and generates the data request signal RQST if the number of the data used for decoding becomes a predetermined number of bits. When new data from FIFO memory 11 is input through decoding interfacer 12 according to the data request signal RQST, decoding unit 13 variable-length-decodes the input data. When the input data cannot be decoded with the internal decoding table during the decoding operation, decoding unit 13 judges that the input data is bit-stuffed data, to then continuously generate data request signal RQST. In more

detail, decoding unit 13 generates data request signal RQST if a sum of the number of the data used for variable-length-decoding and the number of the bit-stuffed data, or the number of the bit-stuffed data becomes the number of the bits for generating data request signal RQST in decoding unit 13. The generated data request signal RQST is output to decoding interfacer 12. In a preferred embodiment of the present invention, the number of the bits for generating data request signal RQST is twenty-four being the number of bits which is read from FIFO memory 11 in a given time. Through such a procedure, the bit-stuffed bits are removed, and are additionally inserted into the rear end of the variable-length-encoded data.

On the other hand, if the data request signal RQST is generated in decoding unit 13 for removing the bit-stuffed bits, decoding interfacer 12 generates a read signal in response to data request signal RQST, and detects the MSC using the data supplied from FIFO memory 11. If the MSC is detected, decoding interfacer 12 stops generation of the read signal and generates a detection resultant signal to supply the generated signal to timing controller 14. Timing controller 14 generates the initialization signal INIT for the following MMB. A point of time of generating the initialization signal INIT is determined based on a point of time of detecting an initially detected FSC, a point of time of detecting the FSC of the previous frame, or a point of time of detecting the MSC of the previous MMB in the Figure 5 apparatus. After the initialization signal INIT is applied from timing controller 14, decoding interfacer 12 generates the read signal in response to data request signal RQST from decoding unit 13. FIFO memory 11 outputs the stored data in response to the read signal to decoding interfacer 12. Decoding interfacer 12 detects the MSC using the data supplied from FIFO memory 11 by the read signal. If the MSC is detected, decoding interfacer 12 outputs the detection resultant signal to timing controller 14 and simultaneously holds the stored data continuously. Decoding interfacer 12 no longer generates the read signal as well. Thus, the variable-length-encoded data in the MMB containing the detected MSC is not applied to decoding unit 13. If timing controller 14 generates a new initialization signal INIT, decoding interfacer 12 reads data from FIFO memory 11 in response to data request signal RQST from decoding unit 13 and supplies the read data to decoding unit 13. From the following operation, a variable-length-decoding operation is performed with respect to fifteen MMBs of one frame through the above-described procedure.

If data is continuously applied from FIFO memory 11 according to the data request signal RQST for reading the bit-stuffed bits filled in the fifteenth MMB, decoding interfacer 12 detects the FSC using the applied data. On the other hand, timing controller 14 generates a new start signal of a frame interval based on the point of time of detecting the previously detected FSC. The start signal is generated at the very previous time when frame head data of a new frame is applied to decoding interfacer 12. Decoding interfacer 12 generates a read signal in response to the start signal. FIFO memory 11 outputs the stored data to decoding interfacer 12 in response to the read signal. If the FSC is detected from the data supplied from FIFO memory 11, decoding interfacer 12 does not generate the read signal any longer and holds the data supplied from FIFO memory 11 as it is. When the FSC is detected, decoding interfacer 12 latches the first MSC in the frame. Thus, decoding interfacer 12 detects the FSC and MSC with respect to the start signal generated every frame except for the initial operation. If the initialization signal INIT is applied from timing controller 14, decoding interfacer 12 performs an operation in which the data from FIFO memory 11 is supplied to decoding unit 13 in response to the data request signal RQST.

On the other hand, during the time when a variable-length-decoding operation is proceeded by the Figure 5 apparatus, decoding unit 13 judges whether EOB data representing the end of every block exists. If the EOB data is not obtained by the decoding operation, decoding unit 13 generates an EOB error signal to supply it to timing controller 14. Decoding unit 13 generates also the data request signal RQST for reading the data of the error-generated MMB. If the EOB error signal is applied, timing controller 14 generates a control signal for interrupting an operation of decoding unit 13 until the detection resultant signal is not applied from decoding interfacer 12. Timing controller 14 generates also a new start signal to output it to decoding interfacer 12. Decoding unit 13 does not decode the data input from decoding interfacer 12 on the basis of the control of timing controller 14. Decoding interfacer 12 continuously reads the stored data from FIFO memory 11 in response to the start signal and detects whether the FSC or MSC exists. Thereafter, in the Figure 5 apparatus, decoding interfacer 12 reads again the data from FIFO memory 11, and performs an operation again between the detection procedure of the FSC or MSC from the read data and the generation procedure of the initialization signal INIT according to the code detection. Thus, when an error is generated in the bitstream, residue data is read until the following MMB data shows up, thereby reconstructing the lost synchronization. Since the following operation is the same as that of normally performing a decoding operation in the Figure 5 apparatus as described above, the detailed description will be

omitted.

Figure 6 is a circuit diagram showing an example of the detailed construction of the decoding interfacer 12 of Figure 5. The FSC used in the Figure 6 apparatus is a hexadecimal value of "00000100H" and the MSC is a hexadecimal value of "000001H". The construction and operation of the Figure 6 apparatus will be described below.

Decoding interfacer 12 comprises a data latch portion 20, an FSC/MSC detector 30, a number output portion 50 and a control signal generator 60. If a high-level pulse start signal or an initialization signal INIT from timing controller 14 is applied to FSC/MSC detector 30 and control signal generator 60, flip-flops 36 and 37 in FSC/MSC detector 30 are cleared by the low-level pulse applied to the reset end via a NOR gate 31, so that the output values are zero. RS flip-flop 61 in control signal generator 60 is cleared by a reset signal /RST and outputs a binary value of "1" via the output end Q in response to the start signal applied to one end S. A flip-flop 65 latches a binary value of "1" applied from RS flip-flop 61 via an OR gate 64. The binary signal latched to flip-flop 65 is output to FIFO memory 11 and flip-flop 66. The binary value of "1" output from flip-flop 65 is used as a read signal for FIFO memory 11. The output of flip-flop 66 is used as a select signal SEL for controlling multiplexers 21, 23, 25, 34 and 35. In data latch portion 20, flip-flops 22, 24 and 26 sequentially latch the data output from FIFO memory 11 by predetermined bits in response to the read signal from control signal generator 60. The data latched in flip-flop 26 is supplied to decoding unit 13. Multiplexer 21 receives the output data from FIFO memory 11 and flip-flop 22, and selects one therebetween according to a binary value of the select signal output from control signal generator 60 to supply the selected one to flip-flop 22. Multiplexer 23 receives the output data from flip-flop 22 and flip-flop 24, and selects one therebetween according to a binary value of the select signal to supply the selected one to flip-flop 24. Likewise, multiplexer 25 receives the output data from flip-flop 24 and flip-flop 26, and selects one therebetween according to a binary value of the select signal to supply the selected one to decoding unit 13. On the other hand, a comparator 32 in FSC/MSC detector 30 compares the output data from flip-flop 22 with the MSC of "000001H". Comparator 32 outputs a binary value of "1" if the data values are the same as each other by the comparison result, while the former outputs a first binary signal having a binary value of "0" if the latter is not different from each other. Multiplexer 34 selects one between the output data of comparator 32 and flip-flop 36 according to the select signal from control signal generator 60 and outputs the selected one to flip-flop 36. The output data from flip-flop 36 is output to flip-flop 38 and control signal generator 60. A comparator 33 compares the data applied to flip-flop 21 with a part of the FSC of "00H". Comparator 33 outputs a binary value of "1" if the data values are the same as each other by the comparison result, while the former outputs a second binary signal having a binary value of "0" if the latter is not different from each other. Multiplexer 35 selects one between the output data of comparator 33 and flip-flop 37 according to the select signal and outputs the selected one to flip-flop 37. The output data from flip-flop 37 is supplied to the inputs of AND gates 39 and 40. AND gate 39 logically multiplies the output data of flip-flops 36 and 37 and supplies the result to number output portion 50. AND gate 40 logically multiplies the inverted output data of flip-flop 36 and the output data from flip-flop 37 and supplies the result to number output portion 50.

On the other hand, RS flip-flop 61 in control signal generator 60 outputs a binary signal of "0" via output end Q in response to a first binary signal, if flip-flop 36 outputs the first binary signal having the value of "1" according to the FSC or MSC detection. AND gate 63 logically multiplies the data request signal RQST from decoding unit 13 by the inverted output data of flip-flop 38, and outputs the result. OR gate 64 logically sums the output data of RS flip-flop 61 and AND gate 63 and outputs the result. Flip-flop 65 latches the output from OR gate 64. The data output from flip-flop 65 is used as a read signal applied to FIFO memory 11. Flip-flop 66 latches the output data from flip-flop 65. The output data from flip-flop 66 is used as select signals SEL for multiplexers 21, 23, 25, 34 and 35.

Number output portion 50 comprises flip-flops 55 and 56 for latching the data applied from flip-flop 24. Multiplexer 53 selects one between the data from flip-flops 55 and 24 according to the output data from AND gate 39 latched in flip-flop 51 and outputs the result to flip-flop 55. Also, multiplexer 54 selects one between the data from flip-flops 56 and 24 according to the output data from AND gate 40 latched in flip-flop 52 and outputs the result to flip-flop 56. Flip-flop 55 latches the frame number and flip-flop 56 latches the MMB number, according to the data selection of multiplexers 53 and 54.

Since it is obvious to a person skilled in the art with respect to the above-described Figure 6 apparatus; thus, the detailed descriptions of the start signal and initialization signal will be omitted. It will be appreciated that the person having ordinary skill can see the Figure 6 apparatus sufficiently based on the Figure 5 apparatus.

As described above, the variable-length-decoding apparatus for the bit-stuffed data according to the present invention synchronizes the data supplied to the decoding unit based on the detection of the FSC and MSC. Thus, although the bit-stuffing is performed on the bitstream, or the error is generated, the MMB following the error-generated MMB can be accurately decoded. As well, when the video frame is processed by dividing the video frame into a plurality of windows, and an amount of the bit-stuffed data is different from each other with respect to the respective windows, the present invention can bring an effect that the synchronization between the windows can be accurately matched.

While only certain embodiments of the invention have been specifically described herein, it will be apparent that numerous modifications may be made thereto without departing from the spirit and scope of the invention.

The reader's attention is directed to all papers and documents which are filed concurrently with or previous to this specification in connection with this application and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference.

All of the features disclosed in this specification (including any accompanying claims, abstract and drawings), and/or all of the steps of any method or process so disclosed, may be combined in any combination, except combinations where at least some of such features and/or steps are mutually exclusive.

Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

The invention is not restricted to the details of the foregoing embodiment(s). The invention extends to any novel one, or any novel combination, of the features disclosed in this specification (including any accompanying claims, abstract and drawings), or to any novel one, or any novel combination, of the steps of any method or process so disclosed.

Claims

1. A variable-length decoding apparatus for variable-length-decoding data transmitted in the form of bitstream after bit-stuffing variable-length-encoded data in each data block to become a predetermined number of bits, and inserting a frame start code representing a start of one frame and a mass of macroblock (MMB) start code for discriminating a plurality of the MMBs contained in one frame from one another, said variable-length decoding apparatus comprising:

a first-in-first-out (FIFO) memory (11) for storing transmitted data and sequentially outputting a predetermined number of bits of data starting from firstly stored bits every time a read signal is input thereto;

decoder means (13) for variable-length-decoding the input data in response to a control signal, generating a data request signal every time the number of bits of the data used for a variable-length-decoding operation becomes a predetermined number of bits, and generating an end of block (EOB) error signal when the EOB data does not exist every block data interval;

decoding interface means (12) for generating the read signal in response to a start signal and the data request signal which is output from the decoder means (13) to then be supplied to the FIFO memory (11), storing the data applied from the FIFO memory (11) according to the read signal by a predetermined number of bits, interrupting generation of the read signal if one of the frame start code and the MMB start code is detected from the input data, and supplying the stored data to the decoder means (13) by a predetermined number of bits if an initialization signal is input; and

a timing controller (14) for generating the start signal every frame interval and the initialization signal every MMB interval to be supplied to the decoding interface means (12), generating a new start signal to be supplied to the decoder means (13) if the EOB error signal is input, and generating a signal for controlling the variable-length-decoding operation to be supplied to the decoder means (13).

2. A variable-length decoding apparatus according to claim 1, wherein said decoding interface means (12) comprises:

a data latch portion (20) of which the data input end is connected to a data output end of said FIFO memory (11), and of which the data output end is connected to said decoding means (13), for latching the data output from said FIFO memory (11) by a predetermined number of bits every read signal, to twice the predetermined number of bits in the input order according to a select signal;

a detector (30) for receiving the data latched to said data latch portion (20) and the data output from said FIFO memory (11), de-

tecting one between the frame start signal and the MMB start signal, latching a first binary signal which is generated to vary the value thereof according to a detection result, and clearing the latched first binary signal if one among the start signal and the initialization signal is input from said timing controller (14); and

a control signal generator (60) for generating the read signal of which the value one between the first binary value for enabling to read the data from said FIFO memory (11) and a second binary value for disabling the read of the data from said FIFO memory (11), and the select signal of which the value is one between a third binary value for newly latching the data supplied from said FIFO memory (11) and a fourth binary value for maintaining the already-latched data as it is.

3. A variable-length decoding apparatus according to claim 2, wherein said data latch portion (20) comprises:

first and second latches (22, 24) for sequentially latching the data output from said FIFO memory (11) by predetermined bits and outputting the latched data to said decoding means (13);

a first multiplexer (21) for receiving the output data from said FIFO memory (11) and said first latch (22) and outputting the received data to said first latch (22) according to a binary value of the select signal; and

a second multiplexer (23) for receiving the output data from said first and second latches (22, 24) and outputting the received data to said second latch (24) according to a binary value of the select signal.

4. A variable-length decoding apparatus according to claim 3, wherein said detector (30) comprises:

third and fourth latches (36, 37) of which the output values are cleared into zero respectively by the start signal and the initialization signal from said timing controller (14);

a first comparator (32) for comparing the output data from said first latch (36) with the predeterminedly set MMB start code, and outputting a first binary signal having a binary value of "1" if the data is identical to each other according to the comparison result while outputting the first binary signal having a binary value of "0" if the data is different from each other according to the comparison result;

a second comparator (33) for comparing the data input to said first multiplexer (21) with a part of the predeterminedly set frame start code, and outputting a second binary signal having a binary value of "1" if the data is identical to each other according to the comparison result while outputting the first binary signal having a binary value of "0" if the data is different from each other according to the comparison result;

a third multiplexer (34) for selecting one between the output data of said third latch (36) and said first comparator (32) according to the select signal and outputting the selected result to said third latch (36);

a fourth multiplexer (35) for selecting one between the output data of said fourth latch (37) and said second comparator (33) according to the select signal and outputting the selected result to said fourth latch (37); and

a fifth latch (38) for latching the output data from said third latch (36).

5. A variable-length decoding apparatus according to any one of claims 2 to 4, wherein said control signal generator (60) comprises:

an RS flip-flop (61) for receiving the start signal from said timing controller (14) via one input end (S) and the first binary signal from said third latch (36) via another input end (R), and outputting the data via the output end (Q);

an AND gate (63) for logically multiplying the data request signal from said decoding means (13) by an inverted output data of said fifth latch (38);

an OR gate (64) for logically summing the output data from said RS flip-flop (61) and the output data from said AND gate (63) and outputting the logically summed result;

a sixth latch (65) for latching the output from said OR gate (64) and outputting the latched result as the read signal applied to said FIFO memory (11); and

a seventh latch (66) for latching the output data from said sixth latch (65) and outputting the latched result as the select signal.

6. A variable-length decoding apparatus according to claim 1, wherein said decoding interface means (12) generates a detection resultant signal if the frame start code is detected and outputting the generated signal to said timing controller (14), and

wherein said timing controller (14) outputs the start signal for the first operation of said variable-length decoding apparatus to said decoding interface means (12), generates a new start signal to read the data containing the MMB start code from said FIFO memory (11) based on a detection resultant signal if the detection resultant signal is applied from said

decoding interface means (12) in response to the start signal for the first operation, and outputs the generated new start signal to said decoding interface means (12).

7. A variable length decoding apparatus comprising means for generating a read signal to output data from a memory means, in which generation of the read signal is interrupted if one of a frame start code or a macroblock code is detected.

8. A variable length decoding apparatus according to claim 7, further comprising any one or more of the features disclosed in the accompanying specification, claims, abstract and/or drawings, in any combination.

FIG. 1 (PRIOR ART)

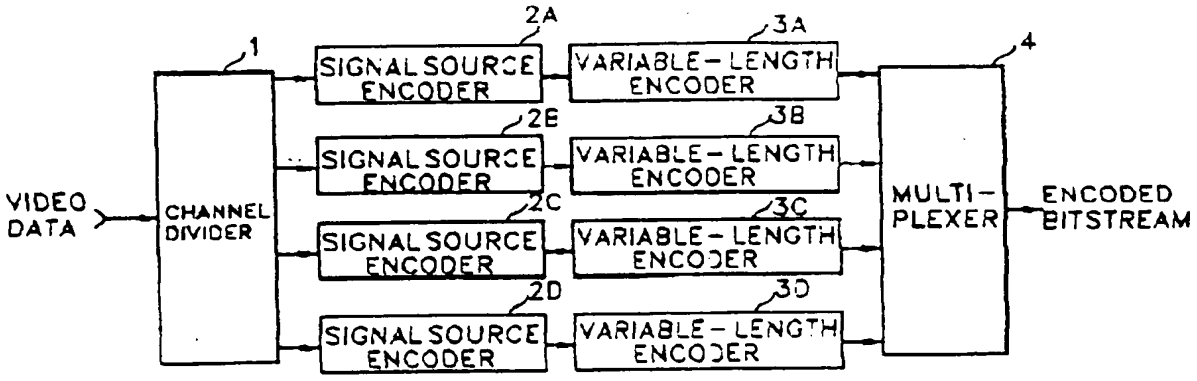

FIG. 2 (PRIOR ART)

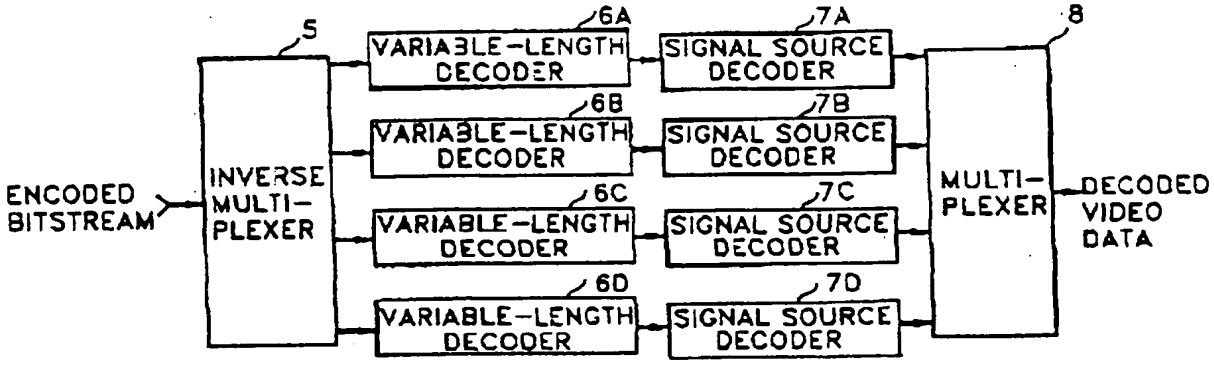

FIG. 4A

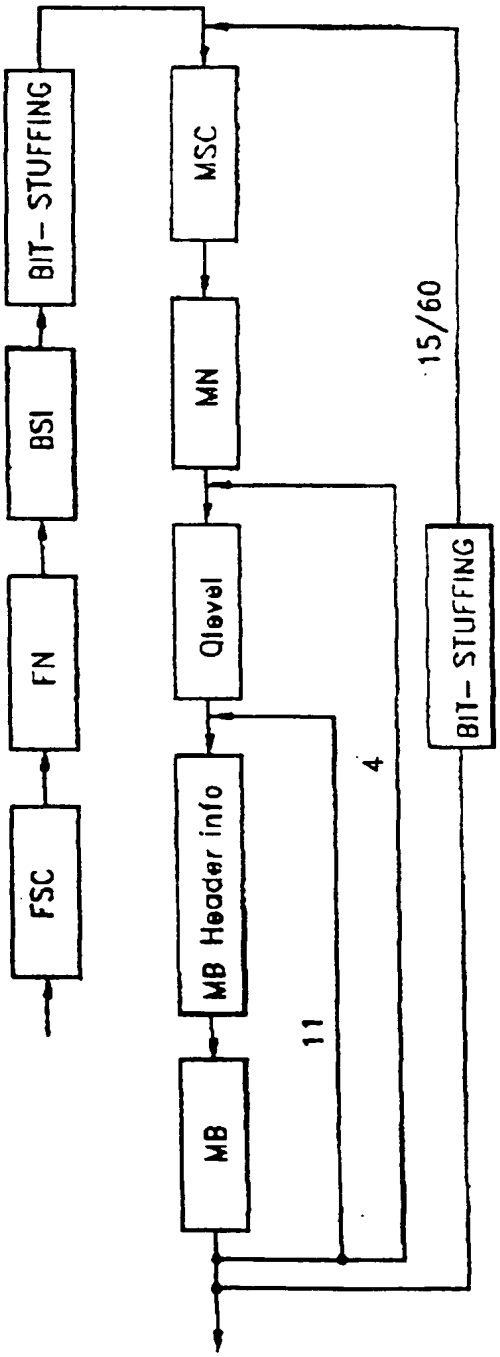
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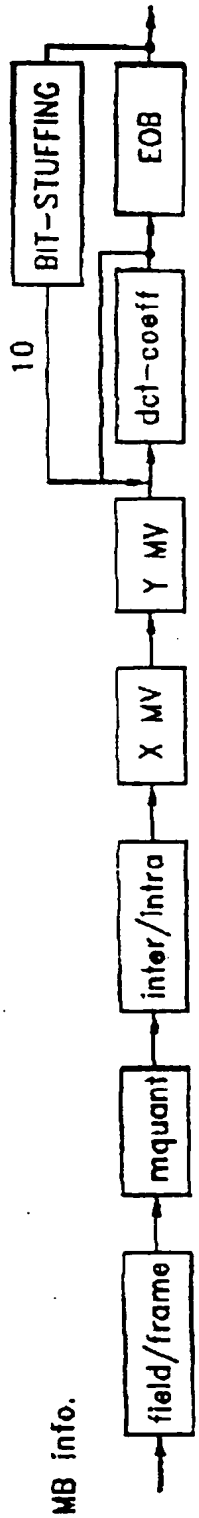
FIG. 4B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Y MV
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EOB
10
BIT-STUFFING

FIG. 3

1ST WINDOW	2ND WINDOW	3RD WINDOW	4TH WINDOW
MMB1	MMB2	MMB3	MMB4
MMB5	MMB6	MMB7	MMB8
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MMB57	MMB58	MMB59	MMB60

FIG. 5

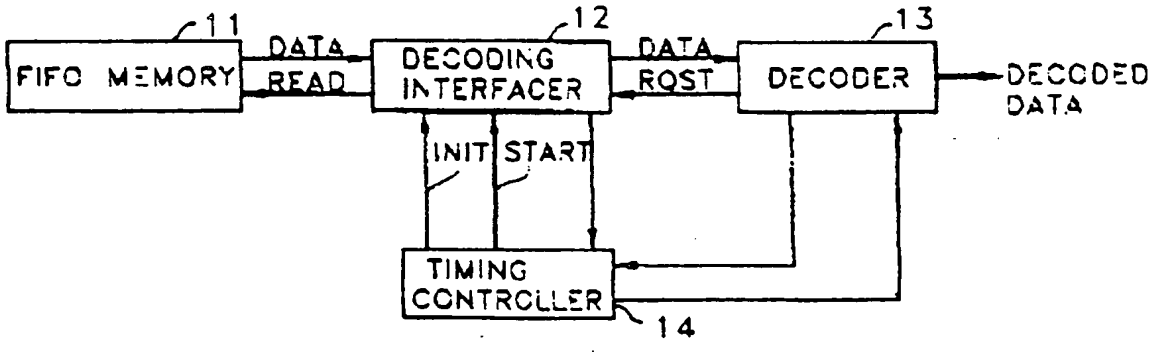
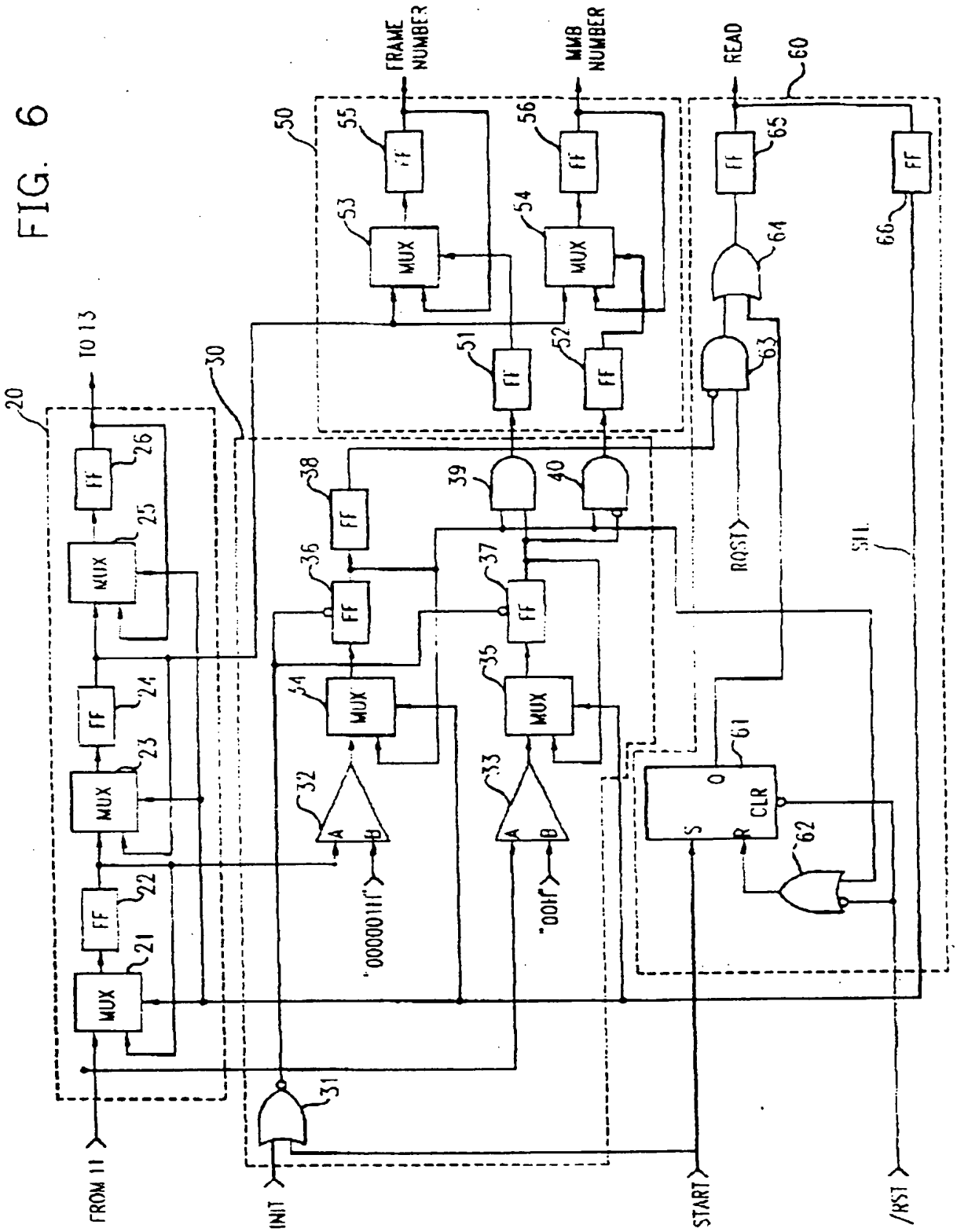


FIG. 6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